ABSTRACT OF THE DISCLOSURE

An apparatus and method are provide for precluding stalls in a microprocessor pipeline due to microcode ROM access delay. The apparatus includes a micro instruction queue and early access logic. The micro instruction queue provides a plurality of queue entries to register logic. Each of the plurality of queue entries includes first micro instructions and a microcode entry point. All of the first micro instructions correspond to an instruction. The microcode entry point is coupled to the first micro instructions. The microcode entry point is configured to point to second micro instructions stored within a microcode ROM. The early access logic is coupled to the micro instruction queue. The early access logic employs the microcode entry point to access the microcode ROM prior to when the each of the plurality of queue entries is provided to the register logic, whereby a first one of the second micro instructions is provided to the register logic when the first one of the second micro instructions is required by the register logic.